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501.39619X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Atsushi SHIMODA et al.

Serial No.: 09/783,604

Filed: February 15, 2001

For: **METHOD FOR ANALYZING CIRCUIT PATTERN DEFECTS AND A SYSTEM THEREOF**

Group: 2623

Examiner: Virginia M. Kibler

SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner of Patents
Washington, D.C. 20231

April 2, 2004

Applicants submit herewith eleven (11) sheets of Formal Drawings in connection with the above-identified application.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
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FIG. 1

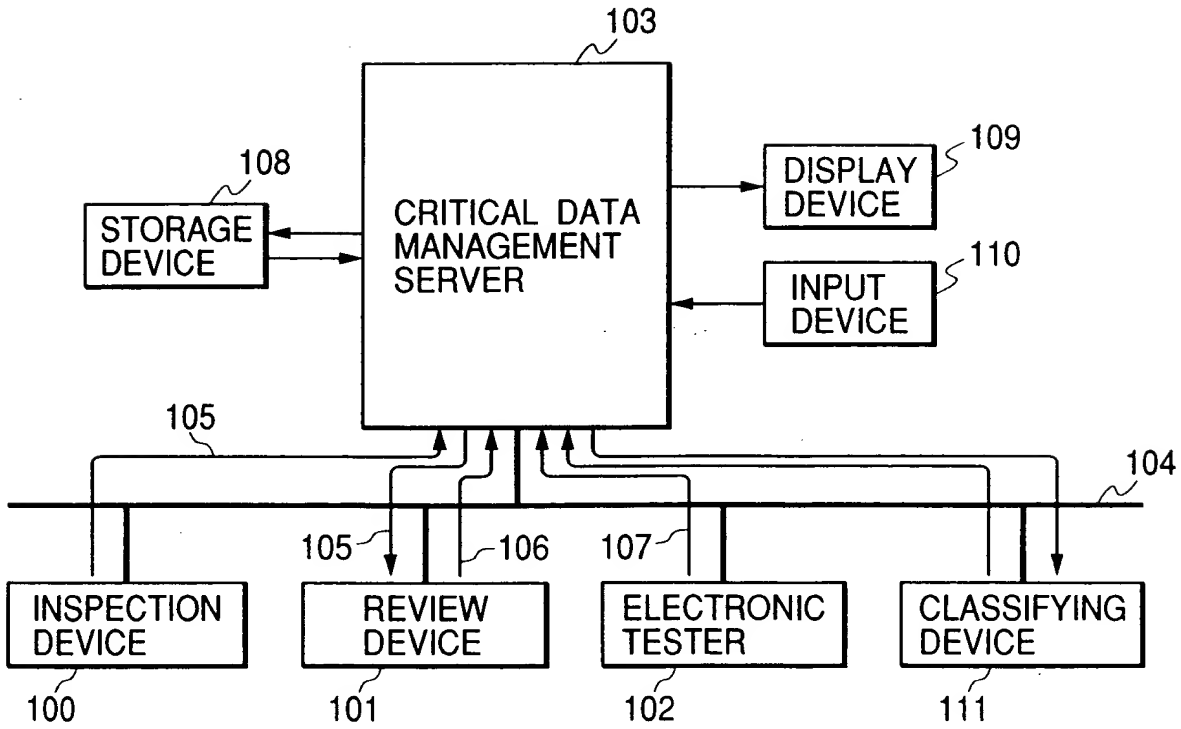

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FIG. 2

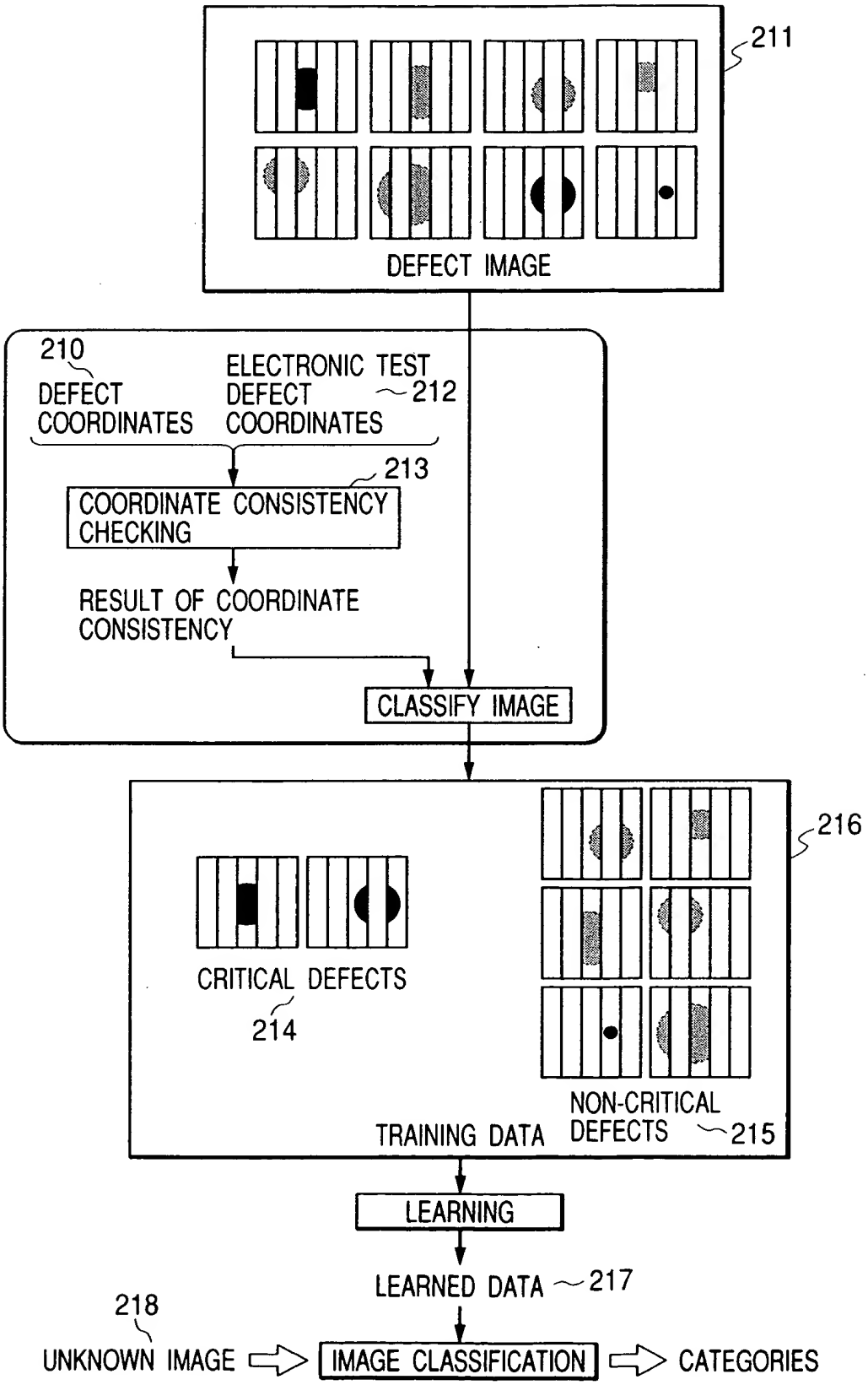

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FIG. 3

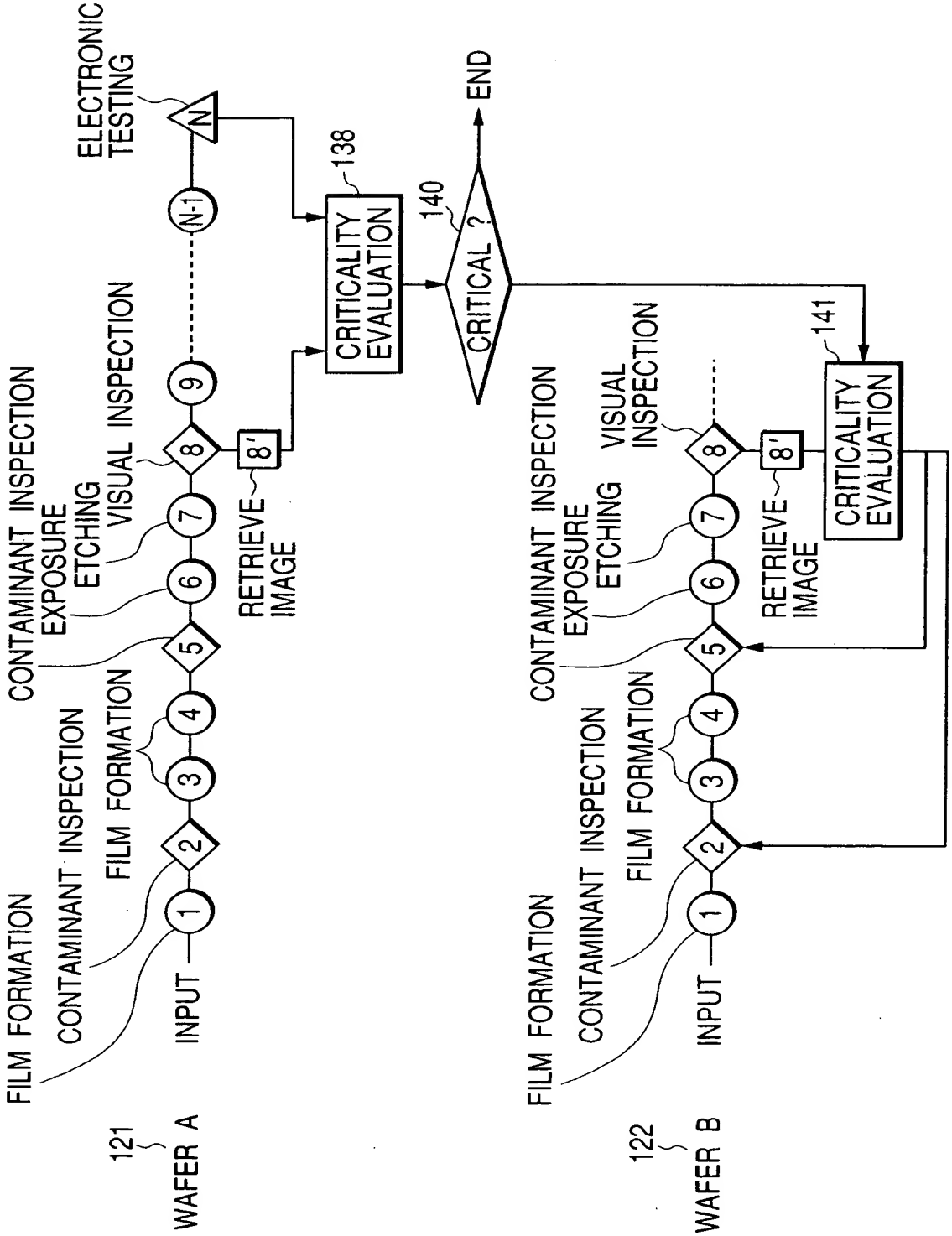

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FIG. 4

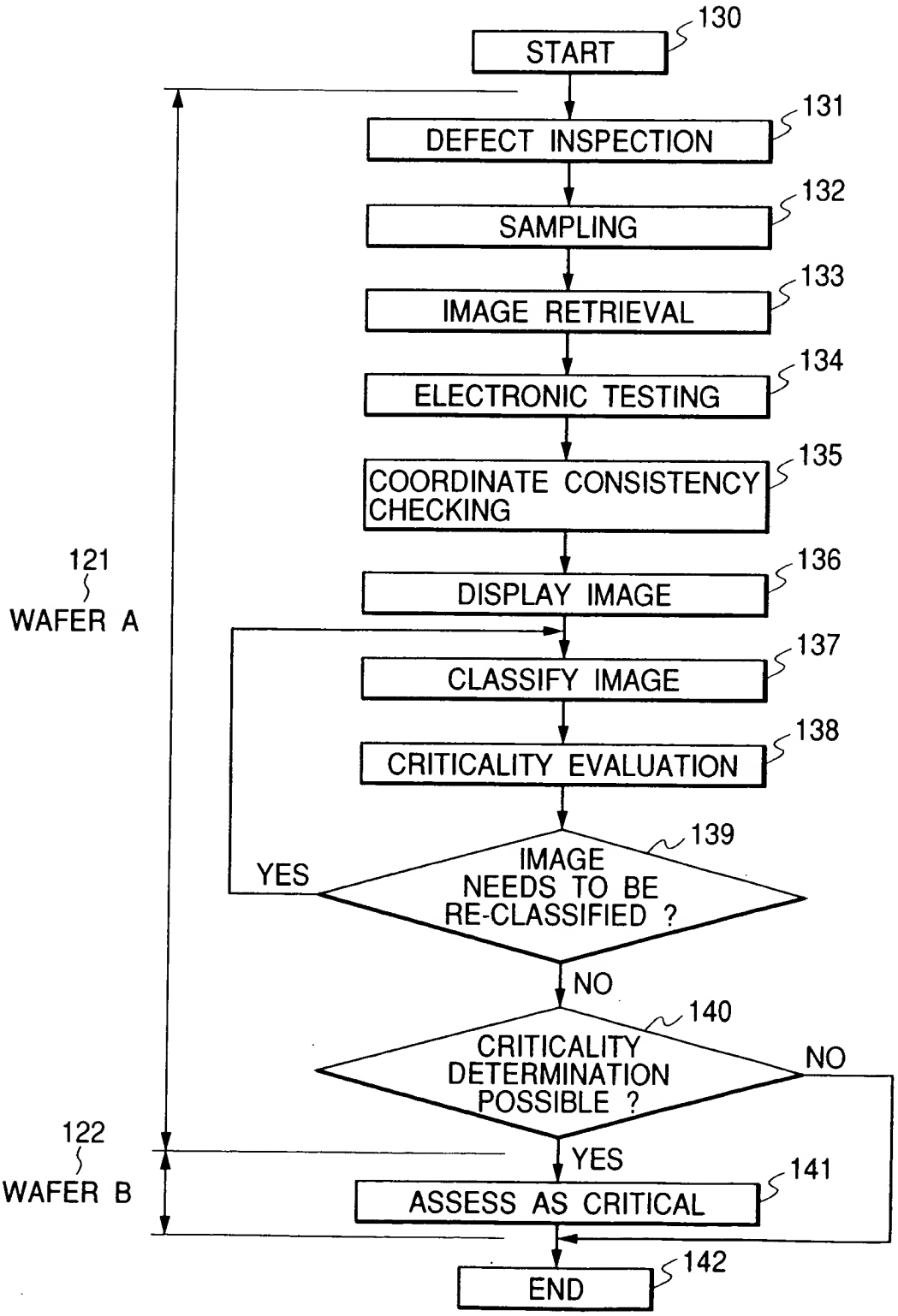

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FIG. 5

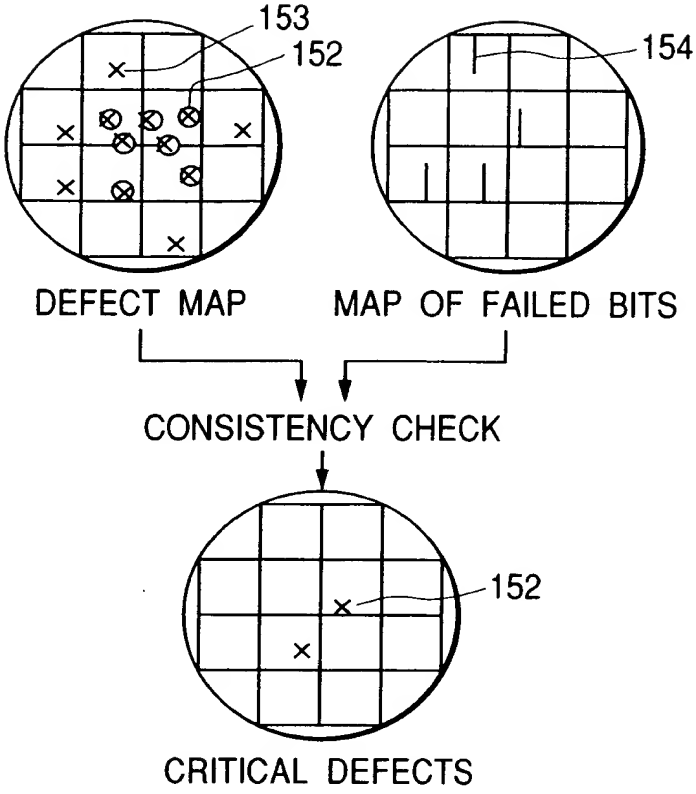

FIG. 6

160 DEFECT NUMBER	161 CHIP COORDINATES	162 DEFECT COORDINATES	163 SAMPLING FLAG	164 IMAGE NAME	165 TEST RESULT
1	(2, 0)	(ΔX1, ΔY1)	0		G
2	(0, 1)	(ΔX2, ΔY2)	0		G
3	(1, 1)	(ΔX3, ΔY3)	1	IMAGE 3	N
4	(2, 1)	(ΔX4, ΔY4)	1	IMAGE 4	N
5	(0, 2)	(ΔX5, ΔY5)	0		G
6	(1, 2)	(ΔX6, ΔY6)	1	IMAGE 6	G
7	(1, 2)	(ΔX7, ΔY7)	1	IMAGE 7	G
8	(1, 2)	(ΔX8, ΔY8)	1	IMAGE 8	G
9	(2, 2)	(ΔX9, ΔY9)	1	IMAGE 9	N
10	(2, 2)	(ΔX10, ΔY10)	1	IMAGE 10	N
11	(3, 2)	(ΔX11, ΔY11)	0		G
12	(1, 3)	(ΔX12, ΔY12)	0		N

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FIG. 7(a)

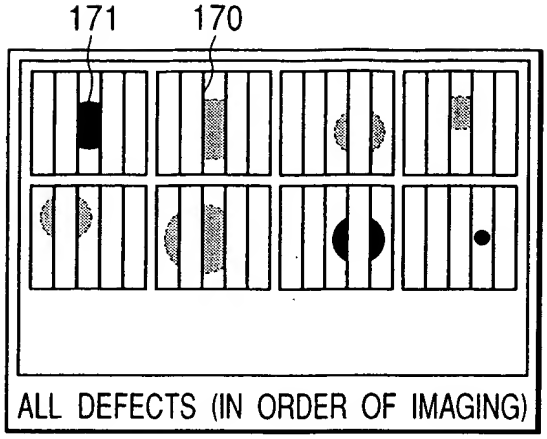

FIG. 7(b)

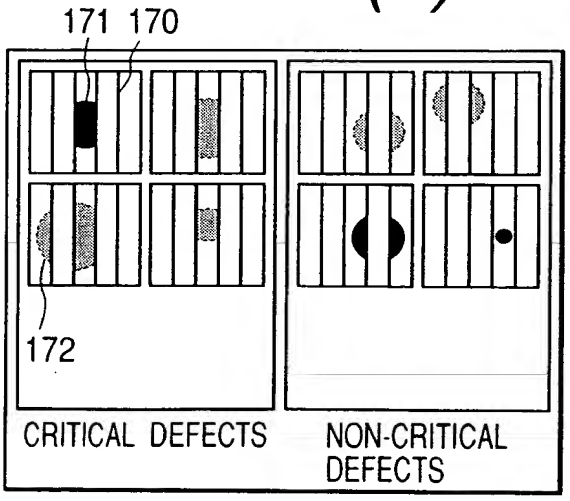

FIG. 7(c)

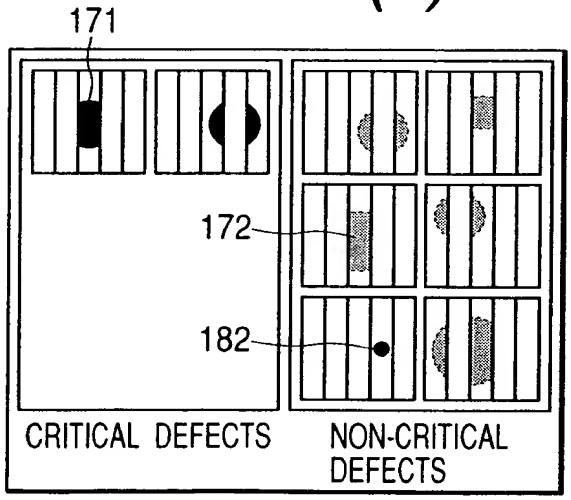

FIG. 9(a)

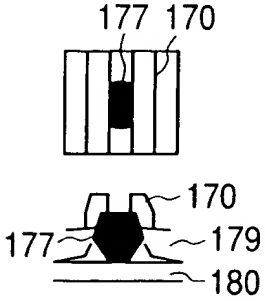

FIG. 9(b)

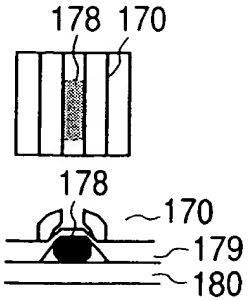

FIG. 9(c)

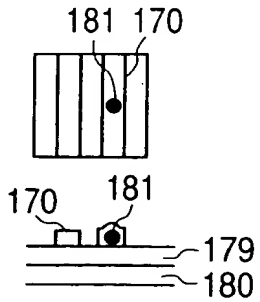

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FIG. 8

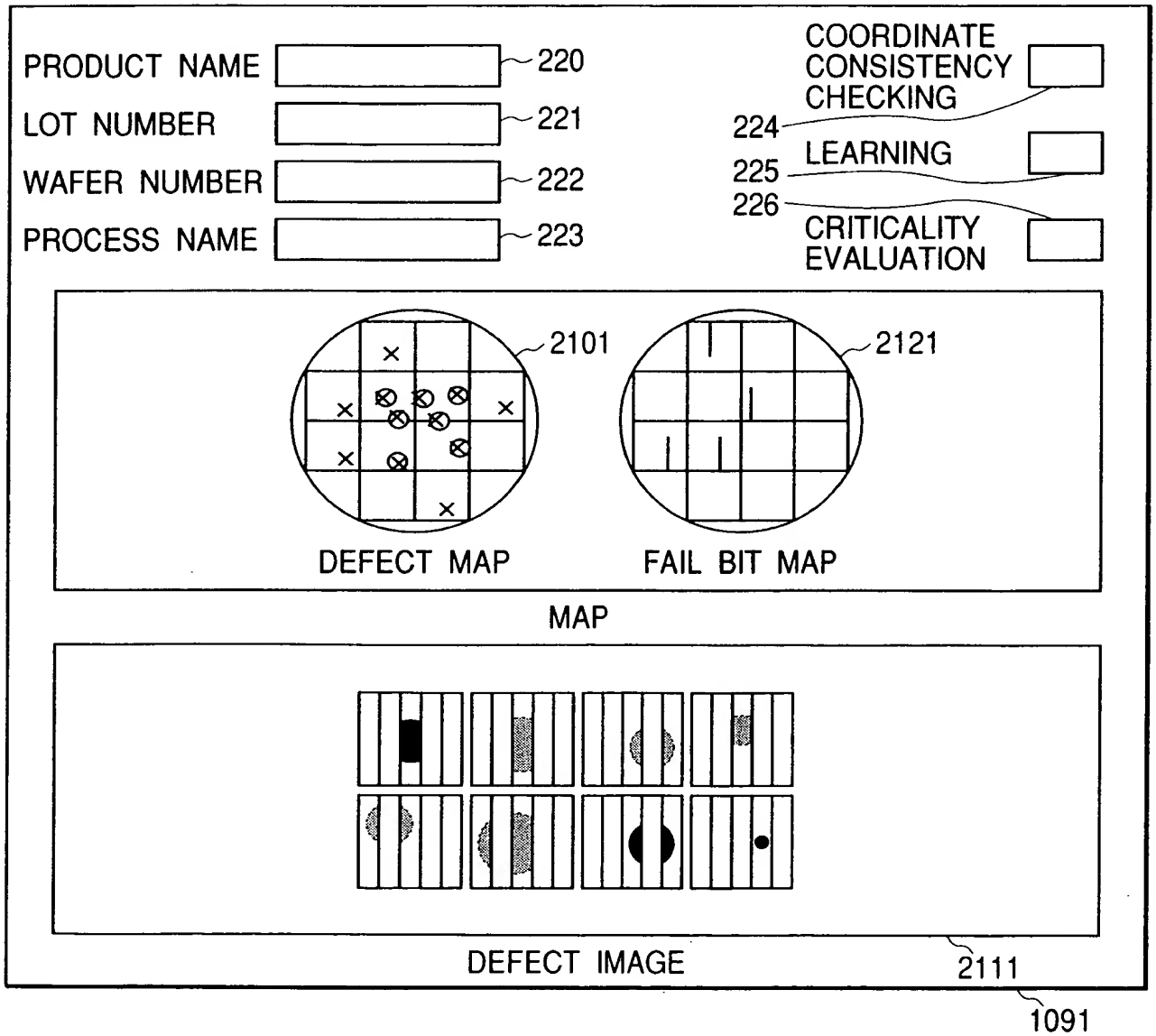

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FIG. 10(a)

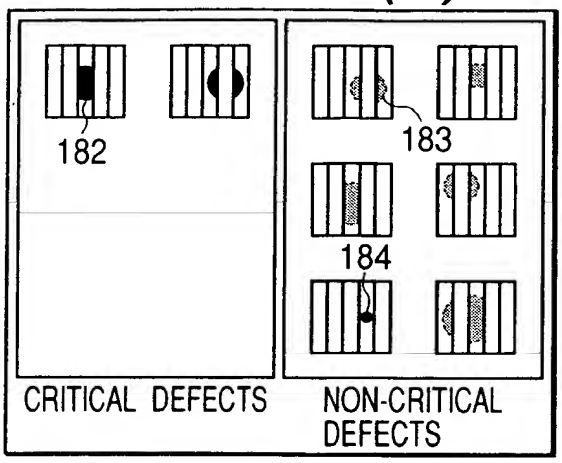

FIG. 10(b)

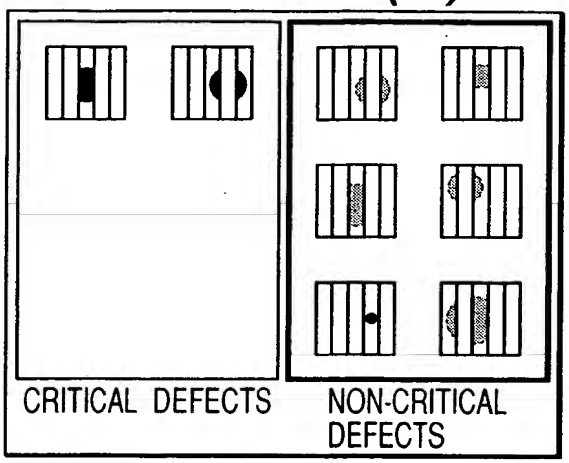

FIG. 10(c)

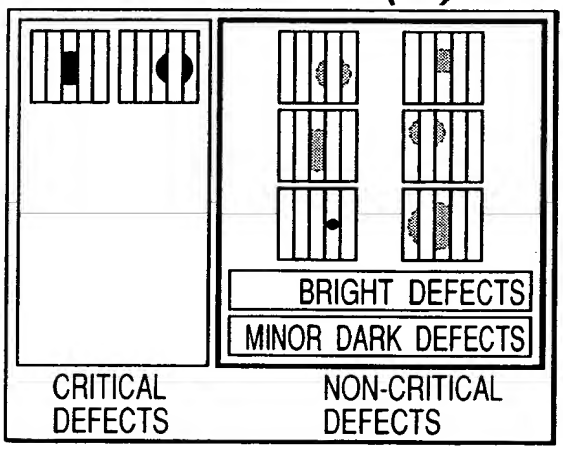

FIG. 10(d)

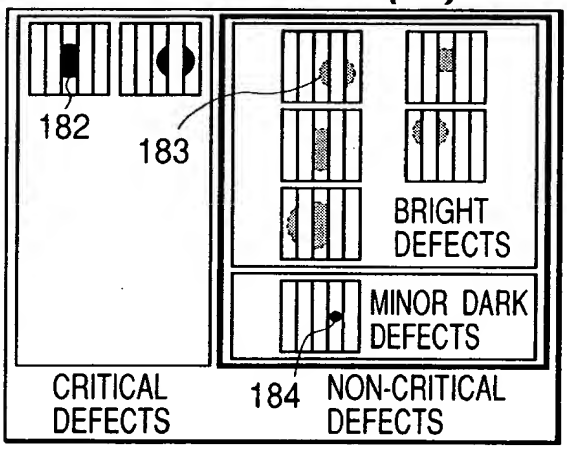

FIG. 11

160 DEFECT NUMBER	161 CHIP COORDINATES	162 DEFECT COORDINATES	163 SAMPLING FLAG	164 IMAGE NAME	165 TEST RESULT	174 IMAGE CLASSIFICATION
1	(2, 0)	(ΔX1, ΔY1)	0		G	G
2	(0, 1)	(ΔX2, ΔY2)	0		G	G
3	(1, 1)	(ΔX3, ΔY3)	1	IMAGE 3	N	N
4	(2, 1)	(ΔX4, ΔY4)	1	IMAGE 4	N	N
5	(0, 2)	(ΔX5, ΔY5)	0		G	G
6	(1, 2)	(ΔX6, ΔY6)	1	IMAGE 6	G	G
7	(1, 2)	(ΔX7, ΔY7)	1	IMAGE 7	G	G
8	(1, 2)	(ΔX8, ΔY8)	1	IMAGE 8	G	G
9	(2, 2)	(ΔX9, ΔY9)	⓪	IMAGE 9	N	N
10	(2, 2)	(ΔX10, ΔY10)	1	IMAGE 10	N	N
11	(3, 2)	(ΔX11, ΔY11)	0		G	G
12	(1, 3)	(ΔX12, ΔY12)	0		N	N

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FIG. 12(a)

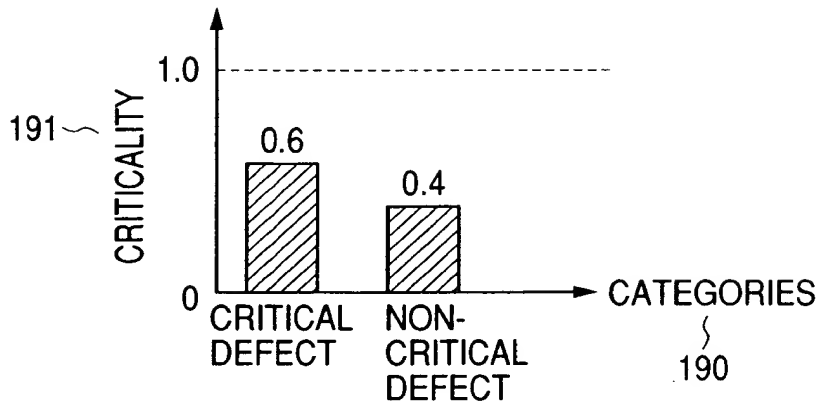

FIG. 12(b)

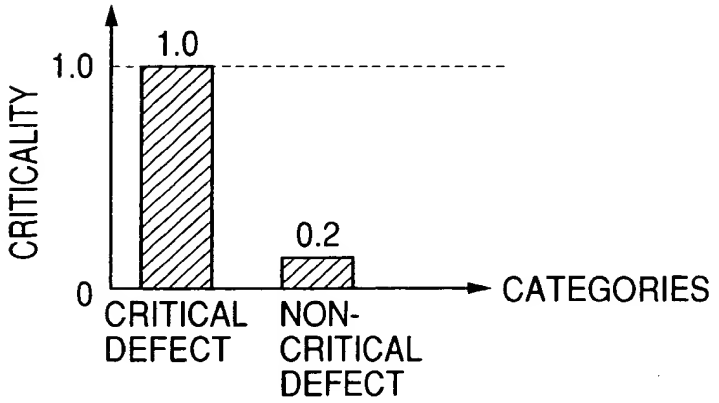

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FIG. 13

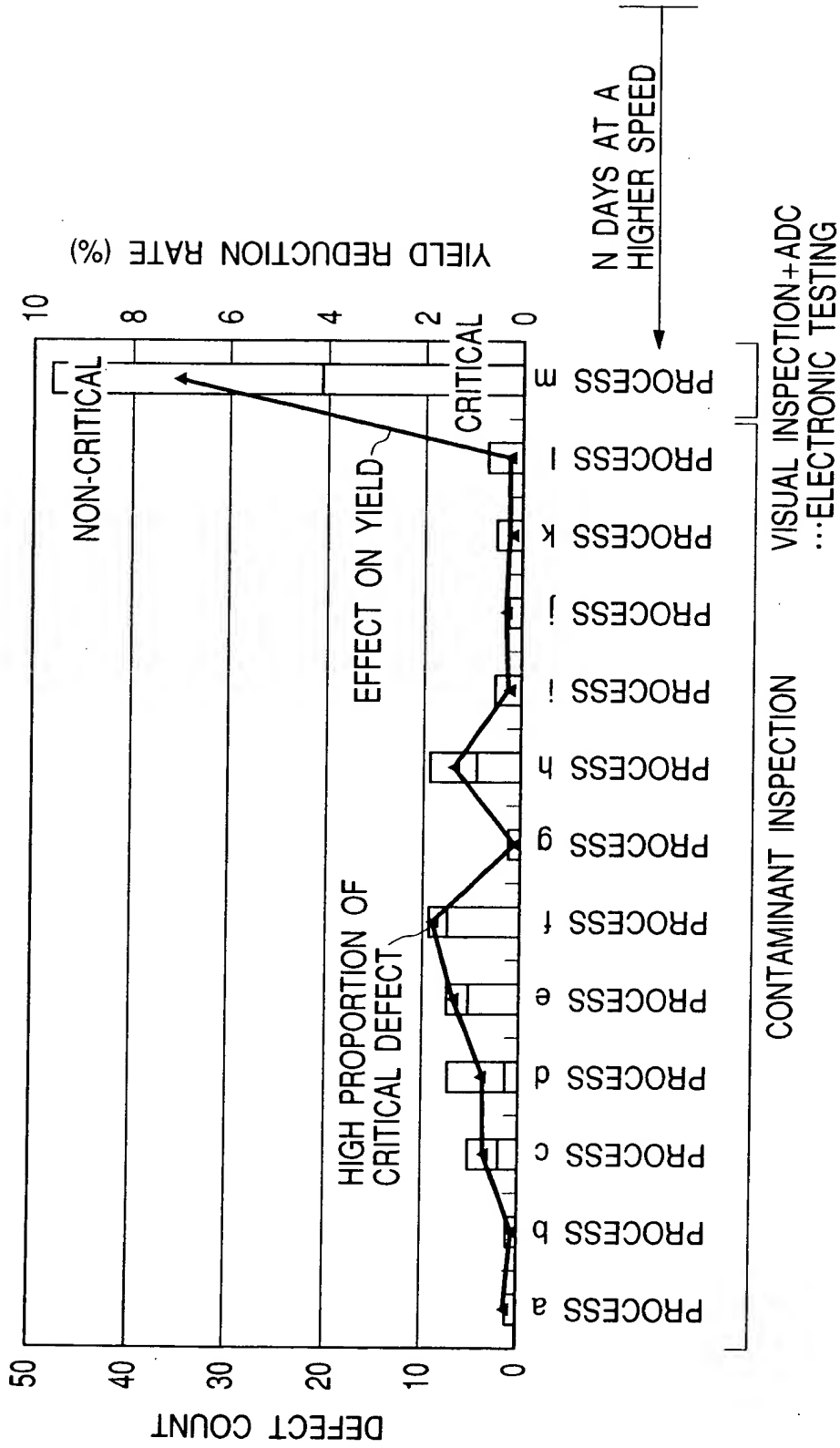

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FIG. 14

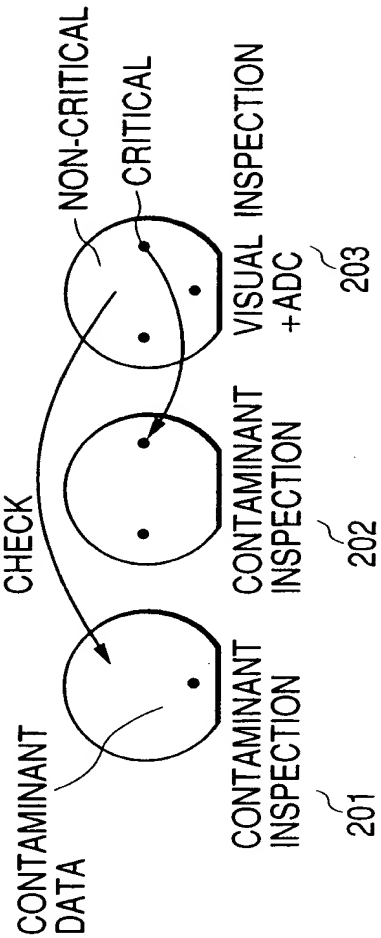
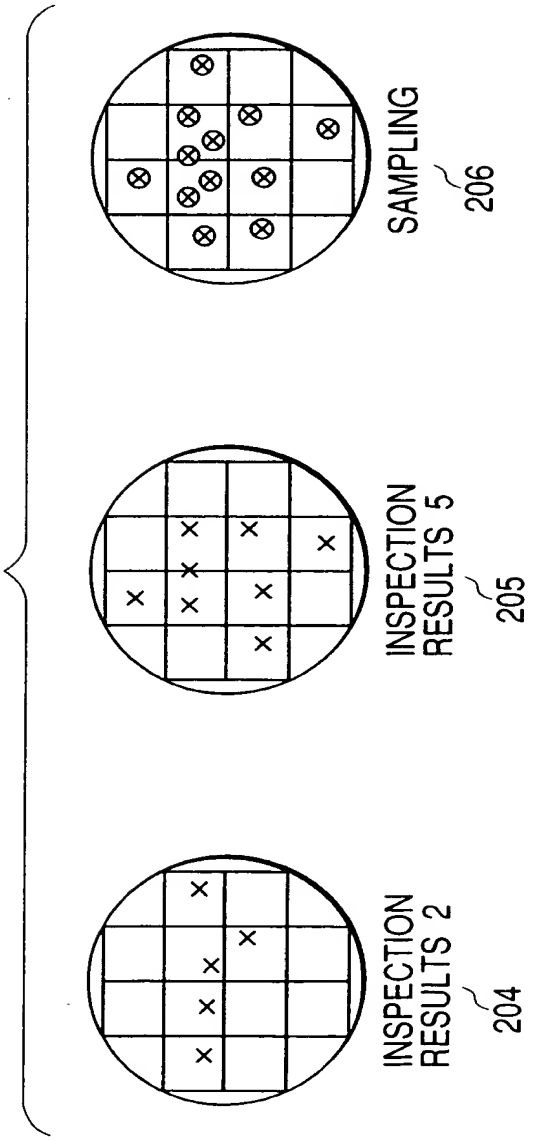
FIG. 15